Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An apparatus, comprising:

a processor; and

a routing agent having logic to change one or more communication pathways in ~~a~~ the processor without changing a physical component layout in the processor based upon a user's input, wherein the processor to implement a protocol having

a protocol layer;

an information transfer layer to electronically transfer information on a physical medium between the protocol layer and a device; and

a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer.

2. (Original) The apparatus of claim 1, wherein the routing agent comprises a first component and a second component, the first component to determine a bandwidth between a device and the processor, the second component to provide a control signal to one or more communication pathway switching devices, the control signal to be based upon the bandwidth determination of the first component.

~~3~~ 4. (Original) The apparatus of claim 1, further comprising:

a point-to-point bus, the processor communicates to a device through the point-to-point bus.

4. (Original) The apparatus of claim 1, wherein the routing agent is internal to the processor.

5. (Original) The apparatus of claim 1, wherein the routing agent is external to the processor.

6. (Original) The apparatus of claim 2, wherein the device is selected from the group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor.

7. (Original) The apparatus of claim 2, wherein the control signal is selected from the group consisting of an enable signal, a disable signal, an increase clock speed signal, or a set default clock speed signal.

8. (Canceled) The apparatus of claim 1, wherein the processor comprises:

a protocol layer;

an information transfer layer to electronically transfer information on a physical medium between the protocol layer and a device; and

a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer.

~~9~~. (Currently Amended) The apparatus of claim ~~8~~1, wherein the one or more communication pathways may be changed by altering a signal path that a signal travels in the information transfer layer.

~~10~~. (Currently Amended) The apparatus of claim ~~8~~1, wherein the one or more communication pathways may be changed by altering a signal path that a signal travels in the buffer layer.

~~11~~. (Currently Amended) The apparatus of claim ~~8~~1, wherein the information transfer layer consists of at least one communication pathway switching device.

~~12~~. (Currently Amended) The apparatus of claim ~~8~~1, wherein the buffer layer consists of at least one communication pathway switching device.

13. (Currently Amended) A method comprising:

receiving an input from a user of a processor to determine an amount of bandwidth between the processor and a device;

sending a control signal to one or more components within ~~a~~ the processor having a flexible architecture; and

changing one or more communication pathways in the processor without changing a physical component layout in the processor.

14. (Original) The method of claim 13, further comprising:

communicating between the processor and a device through at least one point-to-point bus.

15. (Original) The method of claim 13, wherein the changing of the communication pathway consists of changing a setting in a configuration register to direct a routing agent to send the control signal to one or more communication pathway switching devices located in the processor.

16. (Currently Amended) A method comprising:

processing information and generating requests for information in a first layer;

transferring information on a second layer between the first layer and a device external to a processor;

changing a bandwidth between ~~a~~ the processor and ~~a~~ the device external~~exterior~~ to the processor without changing a physical component layout in the processor; and

allowing a user of the processor to select the bandwidth between the processor and the device.

17. (Original) The method of claim 16, further comprising:

communicating between the processor and the device through at least one point-to-point bus.

18. (Original) The method of claim 16, wherein changing the bandwidth comprises altering a number of ports linked between the processor and the device.

19. (Currently Amended) A processor, comprising:

a routing agent having logic to control one or more communication pathways in a processor to determine the bandwidth between the processor and a device, wherein the logic is operable to allow a user of the processor to determine the bandwidth between the processor and the device;

a protocol layer to process information and generate requests for information;

an information transfer layer to transfer information on a physical medium between the protocol layer and ~~a~~ the device; and

a buffer layer to transfer information between the protocol layer and the information transfer layer.

20. (Original) The processor of claim 19, wherein the information transfer layer consists of at least one communication pathway switching device and the buffer layer consists of at least one communication pathway switching device.

21. (Original) The processor of claim 19, wherein the routing agent comprises a first component and a second component, the first component to set a bandwidth between the processor and the device, the second component to send a control signal to at least one communication pathway switching device.

22. (Currently Amended) A system, comprising:

a processor having a flexible packet based protocol architecture having a physical layer, a link layer, and a protocol layer;

a chip connected to the processor via a bus; and

a routing agent having logic to control one or more communication pathways in the processor to determine an amount of bandwidth between the process and the chip, wherein the logic is operable to allow a user of the processor to select the amount of bandwidth between the processor and the chip.

23. (Currently Amended) The system of claim 22, wherein the ~~processor comprises:~~

~~a protocol layer;~~

~~an~~ information transfer layer to transfer information on a physical medium between the protocol layer and a device, wherein the information transfer layer contains a first multiplexer that receives a first signal from the routing agent and a second multiplexer that receives a second signal from the routing agent; and

a buffer layer to buffer the transfer of information between the protocol layer and the information transfer.

24. (Original) The system of claim 22, further comprising:

a point-to-point bus, the processor communicates to a device through the point-to-point bus.

25. (Original) The system of claim 22, wherein the system is selected from a group consisting of a work station, or a server.

26. (Currently Amended) An apparatus, comprising:

a means for changing an amount of ~~the~~ bandwidth between a processor and a device exterior to the processor without changing a physical component layer in the processor; and

a means for allowing a user of the processor to select the amount of bandwidth between the processor and the device.

27. (Original) The apparatus of claim 26, further comprising:

a means for communicating between the processor and the device through at least one point-to-point bus.

28. (Original) The apparatus of claim 26, wherein changing the bandwidth comprises altering a number of ports linked between the processor and the device.

29. (Currently Amended) An apparatus, comprising:

a routing agent having programmable logic to change the bandwidth between a processor and a device exterior to the processor without changing a physical component layer in the processor based upon a user's input.

30. (Original) The apparatus of claim 29, wherein the processor uses a point-to-point bus to communicate with the device.

31. (Currently Amended) The apparatus of claim 29, wherein routing agent further comprises a configuration register to alter a number of ports linked between the processor and the device.

32. (New) The apparatus of claim 1, wherein the logic is a programmable setting in a configuration register located in the routing agent.

33. (New) The apparatus of claim 29, wherein the programmable logic is a configuration register that has a programmable setting.